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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,337	PRITCHARD ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on March 01, 2004. Claims 1-17 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-3,5-7,11-10,16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Inumiya et al (6,054,355).

Re claims 1,16, Inumiya teaches a method for forming an integrated circuit transistor comprising: depositing a first dielectric layer (509 in Fig 1G; 66 in Fig 52B; col 36, line 51 through col 7) on a substrate; etching a gate electrode trench in the first dielectric layer (510 in Fig 1G; 66 in Fig 53B; col 37, lines 12-47); depositing a conformal gate dielectric film to line the trench (512 in Fig 1I; col 1, line 60 through col 2; 69 in Figs 54-56; col 38, lines 1-32); and depositing a gate electrode conductor in the trench to cover the gate dielectric film and fill the trench (513 in Fig 1I; 70 in Figs 55-56). Re claims 16, 16. A method of forming a semiconductor integrated circuit, the method comprising: forming a source and drain diffusion region on a semiconductor substrate (col 36, lines 51 through col 36; Fig 52-56); forming an interlayer dielectric layer (509 in Fig 1G; 66 in Fig 52B; col 36, line 51 through col 7) on the semiconductor substrate after formation of the source and drain diffusions; etching a gate electrode trench in the interlayer dielectric layer (510 in Fig 1G; 66 in Fig 53B; col 37, lines 12-47), the gate electrode trench configured for the placement of a gate electrode to control the current between the source and drain regions; lining the gate electrode trench with a gate dielectric layer (512 in Fig 1I; col 1, line 60 through col 2; 69 in Figs 54-56; col 38, lines 1-32) ; and depositing a gate electrode conductive material in the gate electrode trench after lining the

trench with the gate dielectric film (513 in Fig 1I; 70 in Figs 55-56). Re claims 2,17, wherein the gate electrode trench etch stops on the underlying substrate (Fig 1G; 11G,11H). Re claim 3, wherein the gate electrode trench is extended such that the bottom of the trench forms a depression in the substrate (Figs 54-56). Re claim 5, wherein the gate electrode conductor comprises aluminum (col 4, lines 35-41). Re claim 6, wherein the gate electrode conductor comprises one of aluminum, tungsten, and polysilicon (col 4, lines 35-41; col 38, lines 19-30). Re claim 7, wherein defining a drain and source region in the substrate before depositing the first dielectric layer 66 on the substrate (col 36, lines 51 through col 36; Fig 52-56).
Re claim 10, wherein the first dielectric layer 66 is an interlayer dielectric and further comprising forming at least one contact hole in the first interlayer dielectric (Fig 57-58; col 38, line 30 through col 39). Re claim 11, wherein the at least one contact hole exposes at least one of a source, a drain, or a gate electrode (Figs 57-59); and further comprising forming a salicide (Fig 40F; col 24, lines 40-47) on the exposed at least one of a source, a drain, and a gate electrode.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inumiya et al (6,054,355), as applied above to claims 1-3,5-7,11-10,16-17, in view of Divakaruni (6,501,131).

Inumiya teaches a method for forming an integrated circuit transistor as applied to claims 1-3,5-7,11-10,16-17 above.

Inumiya lacks forming a punch through implant stop layer.

However, Divakaruni et al teach (at Figs 3-4; col 3, lines 28-52) forming a punch through implant stop layer 8 in the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form in a substrate of Inumiya a punch through implant stop layer as taught by Divakaruni. This is because of the desirability to prevent punch through between the source and drain of the device.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inumiya et al (6,054,355), as applied above to claims 1-3,5-7,11-10,16-17, in view of Qiao et al (6,803,318).

Inumiya teaches a method for forming an integrated circuit transistor as applied to claims 1-3,5-7,11-10,16-17 above.

Inumiya lacks mentioning using undoped silicate glass or phosphor-silicate glass for the dielectric layer.

However, Qiao teaches (at col 15, lines 3-51) forming an interlayer dielectric layer of undoped silicate glass or phosphor-silicate glass (PSG).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dielectric layer of Inumiya by using of a layer of undoped silicate glass or phosphor-silicate glass (PSG), as taught by Qiao. This is because these dielectric materials are effective insulating materials for electrical isolating wirings of the device from unwanted interconnection.

6. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inumiya et al (6,054,355), as applied above to claims 1-3,5-7,11-10,16-17, in view of Sugawara (6,750,486) and Ma et al (6,759,695).

Inumiya teaches a method for forming an integrated circuit transistor as applied to claims 1-3,5-7,11-10,16-17 above.

Re claims 12-15, Inumiya lacks mentioning growing a SiGe material in the trench.

However, Sugawara teaches (at Figs 2-4;1; col 4, line 57 through col 6) epitaxially growing a SiGe layer on the channel trench, and a silicon layer thereon. Ma also teaches (at Fig

2; col 3, lines 10-54) epitaxially growing a strained SiGe layer on the substrate, and a silicon layer thereon.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Inumiya by epitaxially growing a SiGe layer on the channel trench, and a silicon layer thereon, as taught by Sugawara and Ma. This is because to enhance high mobility electron or hole channel in strained device.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.
Oacs-18

Michael Trinh
Primary Examiner